ABSTRACT OF THE DISCLOSURE

A clock ride-over circuit in which clock ride-over may be achieved even if jitter is contained in clocks prior to and subsequent to ride-over and no control input signal for write and readout is applied from outside. A clock prior to ride-over CLK_1 is detected by a clock subsequent to ride-over CLK_2 which is of a higher speed than the clock prior to ride-over. A timing signal TIM of a constant period, generated by a counter adapted for self-running with the clock prior to ride-over, is compared to the phase comparison signal COMP which is the result of the clock detection. Stable clock ride-over is possible by the phase comparison signal COMP having a pulse width larger than the jitter period of the clock subsequent to ride-over.